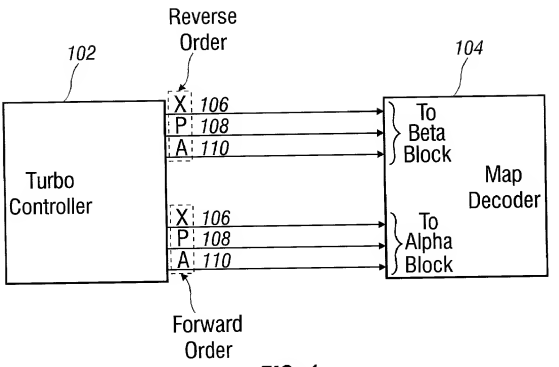
Reverse
Order
102
104
X 106
P 108
A 110
To
Beta
Block
Turbo
Controller
Map
Decoder
X 106
P 108
A 110
To
Alpha
Block
Forward
Order

FIG. 1

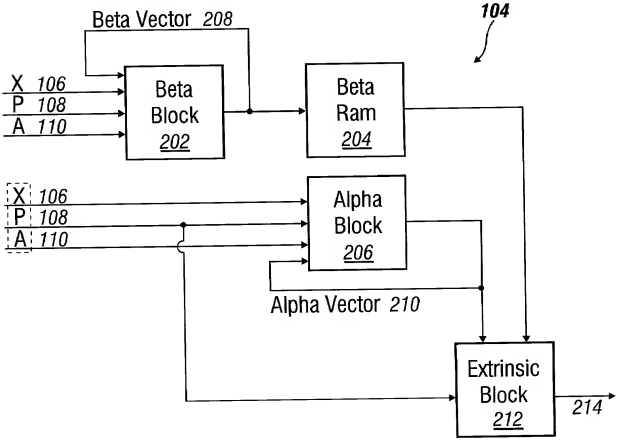
Beta Vector 208
104
X 106
P 108
A 110
Beta
Block
202
Beta
Ram
204
X 106
P 108
A 110
Alpha
Block
206
Alpha Vector 210
Extrinsic
Block
212
214

FIG. 2

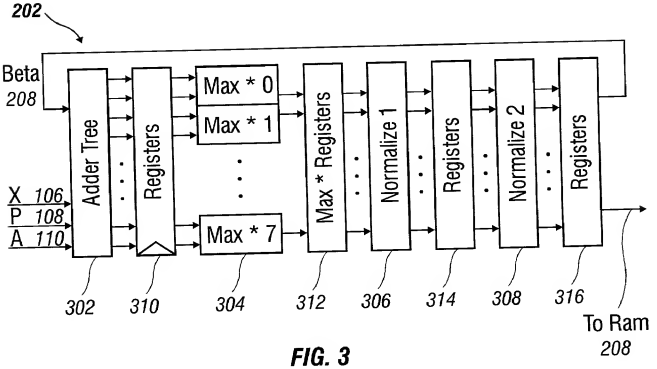
202
Beta
208
X 106
P 108
A 110
Adder Tree
Registers
Max * 0
Max * 1
Max * 7
Max * Registers
Normalize 1
Registers
Normalize 2
Registers
302
310
304
312
306
314
308
316
To Ram
208

FIG. 3

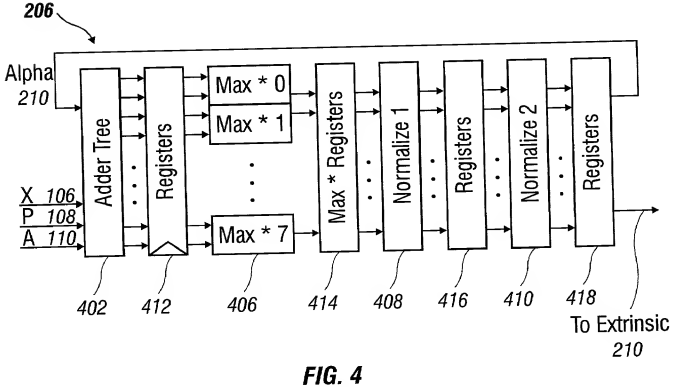
206
Alpha
210
X 106
P 108
A 110
Adder Tree
Registers
Max * 0
Max * 1
Max * 7
Max * Registers
Normalize 1
Registers
Normalize 2
Registers
402
412
406
414
408
416
410
418
To Extrinsic
210

FIG. 4

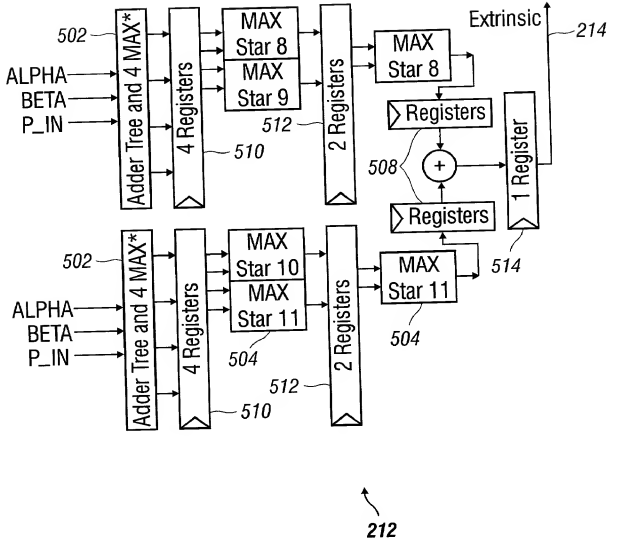
502
ALPHA
BETA
P_IN
Adder Tree and 4 MAX*
4 Registers
MAX Star 8
MAX Star 9
510
512
2 Registers
MAX Star 8
Extrinsic
214
Registers
508
Registers
1 Register
502
ALPHA
BETA
P_IN
Adder Tree and 4 MAX*
4 Registers
MAX Star 10
MAX Star 11
504
510
512
2 Registers
MAX Star 11
504
514
212

FIG. 5

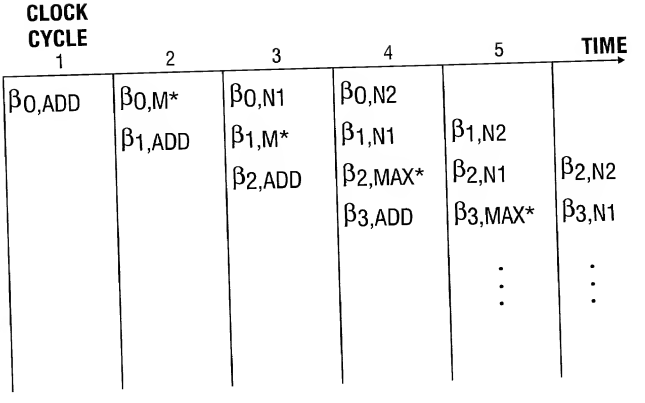
CLOCK CYCLE
1
2
3
4
5
TIME
β0,ADD
β0,M*
β1,ADD
β0,N1
β1,M*
β2,ADD
β0,N2
β1,N1
β2,MAX*
β3,ADD
β1,N2
β2,N1
β3,MAX*
β2,N2
β3,N1

FIG. 6

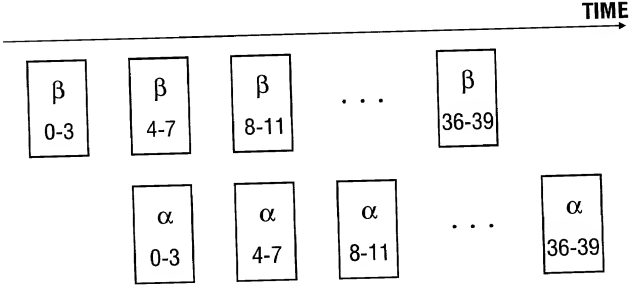
TIME
β 0-3
β 4-7
β 8-11
β 36-39
α 0-3
α 4-7
α 8-11
α 36-39

FIG. 7

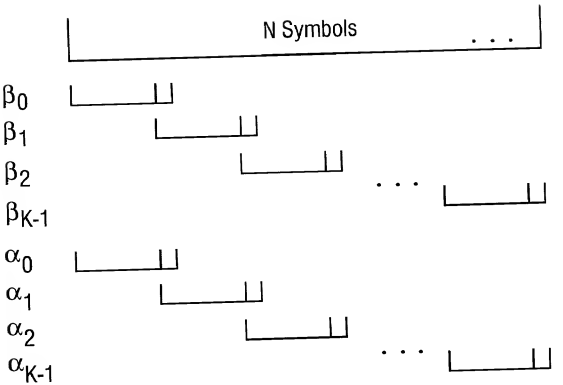

FIG. 8

	Start Prolog	End Prolog	Start Reliability	End Reliability
β_0	123	100	99	0
β_1	223	200	199	100
β_2	323	300	299	200
β_3	423	400	399	300
α_0	N/A	N/A	0	99
α_1	76	99	100	199
α_2	176	199	200	299
α_3	276	299	300	399

FIG. 9